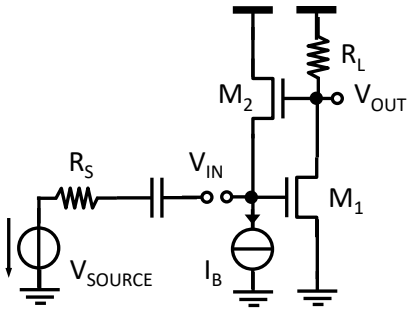
LNA based on a current conveyor

The main goal here is to find a way to impose a well-defined input impedance without the noise associated to a physical resistor leading as we have seen before to a NF of 3dB without providing any RF gain.

An LNA based on a current conveyor is sketched below. It is formed with a gain stage M1 loaded by RL. A feedback path formed with M2 biased with a current source I_B operates as a voltage follower. Let's consider the input node Vin. How is its DC voltage defined? If Vin = 0, M1 is off and Vout = VDD. This leads to a large current in M2 bigger than I_B (by proper design) which charges Vin and start pulling Vout at a lower voltage so that the RL and M1 current are equal. M2 forms thus a negative feedback path setting the DC voltage level Vin so that M1 exactly sinks the RL current. Vin is thus close to M1 threshold voltage depending on its sizing.

Any deviation of Vin, e.g. positive increases the current of M1, lowering Vout thus the current delivered by M2 forcing the circuit to retrieve the equilibrium point. Conversely a negative step on Vin reduces M1 current leading to a Vout raise injecting in turn more current into Vin.

Vout DC voltage is set by M2 since its VGS voltage difference must ensure that M2 exactly delivers I_B. If M2 substrate is at VSS, Vout is close to $VTN_{M1}+n\cdot VTN_{M2}$, n~1.3 being the MOS slope factor. A local bulk connection eliminates the substrate effect. The minimum voltage to operate such a structure is hence $2\cdot VTN+RL\cdot I_{M1}$.



Solving the DC current is interesting to gain insights into the circuit but there are quite a few parameters. It's easier to go directly to the small signal AC analysis with gm1 and gm2 and gms2 and RL (IB is an open circuit in AC). If you neglect all caps, you get a feeling on how the circuit behaves to applied perturbations either at VIN or VOUT (e.g. through a large coupling cap).

Intuitively solving for DC you may start as follow: As a fist guess, you might consider that VIN is close to VT (IC=1) and since this is the source voltage of M2, VOUT is VT+n*VT. Choosing VDD hence gives the current in RL. Then you may solve iteratively the two non-linear equations of VIN; VOUT. But for now, we have no idea on how to split the currents among the two branches and size the transistors.

Deriving the Kirchhoff equations

Let's neglect the RF input for now and consider only the rightmost circuit part.

The circuit has two nodes that we call Vin and Vout (Vo in the equations). For each node we may write that the sum of all small signal currents should be 0. We have thus to find the coefficients a, b, c, d of the following matrix:

$$\begin{pmatrix}0\\0\end{pmatrix}=\begin{pmatrix}a & b\\c & d\end{pmatrix}\cdot\begin{pmatrix}V_{IN}\\V_O\end{pmatrix}$$

By definition, a current entering a device is given the positive sign and vice versa. In AC all voltage source are shorted so VDD is equivalent to GND and all components are in parallel (conductance and susceptance may simply be added).

1) Find the a b c d coefficients (you may neglect caps for all questions below, consider that gm2=gms2 to simplify things and develop your intuitions, then add the n factor, 1/gds is likely greater than RL hence the former could be neglected)
2) Consider the Vo and Vin nodes and calculate Vo/Vin and Vin/Vo with the appropriate above equation (1 at a time !) to understand how the circuit work. In other words how a small perturbation on Vout or Vin affects Vin or Vout in open loop mode
3) Compute the circuit input impedance by injecting a parametric current Iin at the input node and determine the input matching conditions
4) Similarly compute the output impedance
5) Compute the transimpedance gain of the circuit from Iin to Vout
6) Compute the input referred noise and the output one.
7) Assuming input match, calculate the voltage tranfer function from VS to VOUT
8) You may know include RS into the set of equations and recalculate the output impedance
9) With Rs (thus the modified equations set) calculate the noise factor F of the circuit assuming that the input matching is satisfied to simplify your solution